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Gilbert-Cell Mixer for WiMAX Applications

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Author's contribution

The sole author designed, analyzed, interpreted and prepared the manuscript.

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ABSTRACT

Differential implementation is becoming highly popular in Radio Frequency Integrated Circuit (RFIC) design, notably for its high immunity to common-mode noises, acceptable rejection of parasitic coupling, and increased dynamic range. One RF front-end building block that is usually designed as a differential circuit is the mixer. This paper presents a design, study, and optimization of a differential mixer, more specifically the Gilbert-cell mixer (also known as double-balanced mixer) implemented on a direct-conversion architecture in a standard 90 nm Complementary Metal-Oxide Semiconductor (CMOS) process. Operating frequency is set to 5GHz, which is a typical frequency for Worldwide Interoperability for Microwave Access (WiMAX) receiver. Impedance matching was necessary to design and fully optimize the mixer design. The direct-conversion Gilbert-cell mixer design ultimately achieved conversion gain of 11.463dB and noise figure of 16.529dB, comparable to mixer designs from past research and studies.

Keywords: Gilbert-cell mixer; direct-conversion; conversion gain; noise figure; WiMAX.

1. INTRODUCTION

The front-end of a Radio Frequency (RF) wireless receiver is of particular interest to many

RF Integrated Circuit (IC) designers and researchers as it attests to be the most critical part in many communication systems and wireless applications like the Bluetooth, Wireless

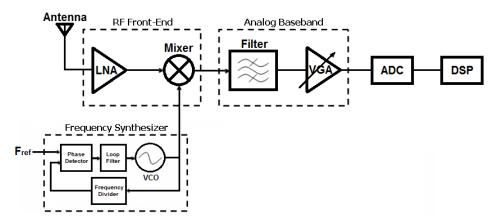


Fig. 1. Block diagram of a typical wireless receiver

Fidelity (WiFi), and Worldwide Interoperability for Microwave Access (WiMAX). The block diagram of a typical RF or wireless receiver is shown in Fig. 1.

Mixer is among the front-end building blocks of an RF receiver. It is also referred to as a converter because it converts RF signals into a lower Intermediate Frequency (IF) by mixing with an offset Local Oscillator (LO). Depending on the RF receiver requirements, mixers must undergo a careful design process since complex tradeoffs exists among different performance parameters. For this paper, the objective is then to design and optimize a direct-conversion Gilbert-cell (or double-balanced) mixer implemented in a standard 90 nm Complementary Metal-Oxide Semiconductor (CMOS) process. Operating frequency is set to 5GHz, which is a typical frequency for an RF receiver particularly the WiMAX receiver.

2. LITERATURE REVIEW

Receivers can be categorized as high-IF, low-IF, and zero-IF or direct-conversion based on the resulting IF signal they operate. For the direct-conversion receiver, IF is designed to be centred at DC (direct current) or zero frequency. This

indicates that the LO frequency is equal to the input RF frequency. With zero-IF, image signal is avoided and the analog filtering problem can be easily handled. Moreover, the desired signal is translated directly to the baseband, allowing Analog-to-Digital Converter (ADC) and Digital Signal Processing (DSP) circuits to perform modulation and other auxiliary functions [1]. This eliminates the need for highly complex filters since channel selection only requires a Low-Pass Filter (LPF) as shown in Fig. 2. Smaller and cheaper receivers with low power consumption could be realized for various wireless applications such as Bluetooth, WiFi, and WiMAX. Many of the implemented receivers in WiMAX [2,3] use the zero-IF architecture since the LPFs make sure that the closely-spaced carrier signals do not cause interference with each other.

Designing a mixer must take into consideration the tradeoffs among the performance parameters. As previously mentioned, a careful study of these important parameters must be done in order to design a fully-functional and optimized mixer. A mixer's efficiency on frequency conversion from RF to IF is characterized by conversion gain (CG) or loss, expressed in Eq. (1) and (2). CG is the ratio of

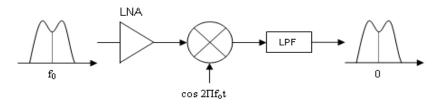


Fig. 2. Direct-conversion or zero-IF receiver

the desired IF output to the value of the RF input, and may be expressed in voltage or power. In cases when conversion gain is less than unity or 0dB, it is appropriately termed as a conversion loss.

$$CG_{voltage} = 20log \frac{V_{IF}}{V_{RF}}$$
 Eq. (1)

$$CG_{power} = 10log \frac{P_{IF}}{P_{RF}}$$
 Eq. (2)

 $V_{\rm IF}$ and $V_{\rm RF}$ are the root mean square (RMS) voltages of the IF and RF signals, respectively, while $P_{\rm IF}$ and $P_{\rm RF}$ are the equivalent power of the IF and RF signals, respectively. Conversion gain is preferred over conversion loss because amplification along with frequency translation. Nonetheless, it should be noted that conversion gain directly affects the noise figure and linearity of the overall receiver. Hence, design tradeoffs concerning these parameters are inevitable.

Noise figure (NF) is another important parameter of the mixer. It is a measure of the amount of signal-to-noise-ratio (SNR) degradation introduced by the mixer as seen at the output. Eq. (3) shows the relation between the SNR at

the input port (SNR_{IN}) and the SNR at the output port (SNR_{OUT}) of the mixer.

$$NF = 10log\left(\frac{SNR_{IN}}{SNR_{OUT}}\right)$$
 Eq. (3)

Noise figures of mixers tend to be higher than amplifiers (i.e. low-noise amplifiers, power amplifiers) because of the noise contribution of preceding building blocks and the noise generated from stray and nearby frequencies (apart from input RF signal) that can mix down to the IF. This considerable noise in mixers is the main reason why Low-Noise Amplifiers (LNA) are used in the front-end, before the mixer [4].

A popular solution for the mixer is based on the double-balanced topology, with the schematic shown in Fig. 3. Double-balanced mixer is also commonly known as Gilbert-cell mixer. It operates with differential LO and RF inputs. In this topology, LO products are prevented from getting to the output by combining two single-balanced mixers. As illustrated in Fig. 3, the two single-balanced mixers are connected in antiparallel as far as the LO is concerned, but in parallel for the RF signal. Thus, the LO terms sum to zero in the output, whereas the converted RF signal is doubled in the output [4,5]. This is most desirable for high port-to-port isolation and spurious output rejection applications.

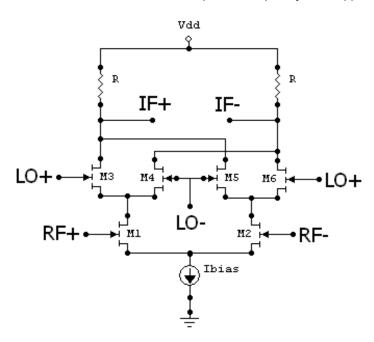


Fig. 3. Gilbert-cell mixer or double-balanced mixer configuration

Table 1. Performance comparison of mixer designs

Reference design	RF (GHz)	Conversion gain (dB)	Noise figure (dB)	Topology
[3]	2~11	21.5~22.8	21.5~25.8	Double-balanced
[5]	3.4~3.85	10	10	Single-balanced
[7]	2	19.5	10.2	BiCMOS Double-balanced
[8]	20~40	16		BiCMOS Single-balanced
[9]	5.2	9.3	10.5	Double-balanced

As earlier mentioned, the goal of the paper is then to design and optimize a direct-conversion Gilbert-cell mixer implemented in a standard 90 nm CMOS process, operating at frequency of 5GHz which is a typical frequency for a WiMAX receiver. The target specifications of the figures of merit are based on the performance comparison in terms of conversion gain and noise figure of past researches on direct-conversion active mixer topologies given in Table 1.

3. DESIGN OF GILBERT-CELL MIXER

Gilbert-cell or double-balanced mixer topology can provide high conversion gain, very low noise figure, and a high degree of LO-IF isolation. The main disadvantage of this topology is its physical implementation. A balun transformer is required to convert the single-ended input to a differential RF input signal of the mixer. The use of active baluns instead of their passive counterparts offers an advantageous solution as they can produce gain, occupy smaller chip area and can operate at RF and higher frequencies [6].

Shown in Fig. 4 is the schematic design of the Gilbert-cell mixer. It is important to determine the proper biasing and sizing of all the transistors such that RF transistors (M1-M2) will operate in the saturation region while the LO transistors (M3-M6) operate near the boundary of the saturation and linear regions. The mixer design used NMOS standard Vt (nsvt), which is the typical model for the transistor.

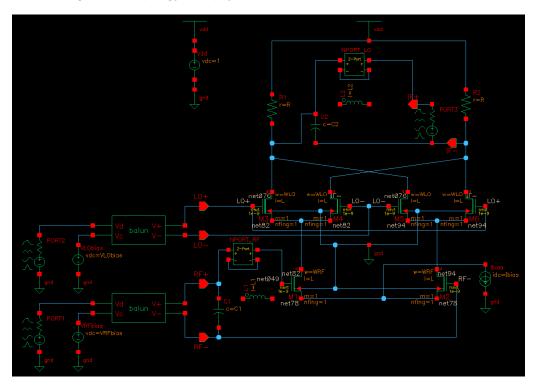


Fig. 4. Schematic design of Gilbert-cell mixer

One way to increase the performance of the mixer in terms of conversion gain and noise figure is to apply impedance matching in the circuit. Input impedances Z_{11} and Z_{22} can be obtained using S-Parameter (SP) analysis which is swept from frequency f_1 = 700MHz to f_2 = 6GHz. Actual inductor and capacitor values at frequency f = 5GHz can be computed from the L-network reactances.

To supply differential LO input to the mixer, a port PORT2 with a matching resistor (set to 50Ω) is used which is then fed into an ideal passive balun to convert the single-ended signal into differential. For the differential RF input of the mixer, same setup as the LO is used with PORT1. To use the differential output for measurements, matching the IF output port PORT3 to the output impedance of the mixer is necessary. PORT1 is set to DC source type with Periodic AC Magnitude (pacmag) set to 1. PORT3, which is the IF port, is set also to DC source type. The only large signal is from PORT2 which is a sine wave with $f_{LO} = 5 \text{GHz}$ and $P_{LO} = 0 \text{dBm}$.

For the impedance matching, the input matching network is applied before the differential RF input of the mixer instead of placing it before the balun. Impedance matching is essential in RF circuit design to provide maximum possible power transfer between the source or the generator and the load [1,10]. This will result to an adjustment on the value of L₁, which will decrease, since the balun circuit has self-inductance. The adjusted value of L₁ can be determined using the SP analysis swept from f₁ = 700MHz to f₂ = 6GHz. Moreover, inductors with small inductances are more realizable in actual designs than their larger counterparts. The final values of the L-matching network are summarized in Table 2.

Table 2. Performance comparison of mixer designs of past researches

L and C	Value
L_1	12.7 nH
C_1	1.116 pF
L_2	1.329 nH
C_2	267.127 fF

Software design tools namely Analysis and Simulation of Spiral Inductors and Transformers for ICs (ASITIC) [11,12] and Integrated Spiral Inductor Calculator (SpiralCalc) [13,14] are used for the design of the inductors. Both tools are

available for academic and non-commercial purposes. Table 3 shows the design parameters obtained for the design of the spiral inductors using ASITIC while Table 4 shows that of using SpiralCalc.

Table 3. Inductor design using ASITIC

Design	Inductors		
parameters	L ₁	L ₂	
Desired L	12.7 nH	1.329 nH	
No. of sides	4	8	
Length, D	300 µm	190 µm	
Metal width, W	10.886 µm	10.902 μm	
Spacing, S	1	1	
No. of turns, N	4.25	2.5	
Metal layer	7	7	
Inductance, L	12.711 nH	1.329 nH	
Q-factor, Q	2.322	5.694	

Table 4. Inductor design using SpiralCalc

Design	Inductors		
parameters	<i>L</i> ₁	L ₂	
Desired L	12.7 nH	1.329 nH	
No. of sides	4	8	
Length, D	300 µm	190 µm	
Metal width, W	11.2 µm	10 µm	
Spacing, S	1	1	
No. of turns, N	6	2	
Inductance, L:			
Modified Wheeler	12.885 µm	1.326 µm	
Current Sheet	12.739 µm	1.326 µm	
Monomial Fit	12.624 µm	1.394 µm	

In ASITIC, the spiral inductors are designed such that desired inductances are achieved and the Q-factors are optimised with the eddy-current option enabled to include the effects of substrate-induced eddy current losses. Inductor L_1 has smaller Q-factor than L_2 because of its high inductance value. For the inductor design using SpiralCalc, same parameter values from the ASITIC parameters are used except for the metal width and the number of turns of the spiral inductor. These parameters are tweaked such that the desired inductances are achieved for the inductors.

The n2port from the analogLib library is used as a model block for all the ASITIC inductors. Touchstone format of S-parameter file is used as file input of the n2port component since the actual S-parameters using ASITIC are given in touchstone format. The figures of merit such as conversion gain and noise figure are determined

using SpectreRF in the Analog Design Environment.

4. RESULTS AND ANALYSIS

A mixer's frequency converting action is characterised by conversion gain or loss. Voltage conversion gain is the ratio of the RMS voltages of the IF and RF signals, earlier given in Eq. (1). The variations of conversion gain with the power of LO signal (P_{LO}) can be measured using swept Periodic Steady-State (PSS)

analysis with Periodic AC (PAC) analysis. The PAC analysis will then compute the voltage conversion gain in dB20 of the whole circuit with PORT3 as the output port (with output harmonic of 0, which is 5GHz) and PORT1 as the input port (with input harmonic of -1, which is 0GHz). Setting the input port to RF+ port, which is located after the balun circuit, will compute the voltage conversion gain of the mixer only. Simulation plots of the conversion gain swept from P_{LO} = -10dBm to P_{LO} = 30dBm are shown in Figs. 5-7.

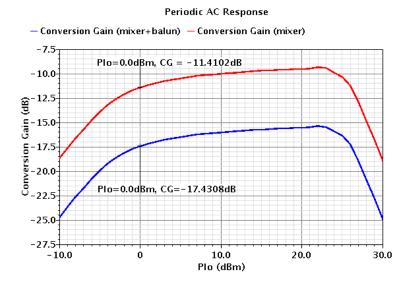


Fig. 5. Conversion gain (in dB) vs. PLO (w/o matching)

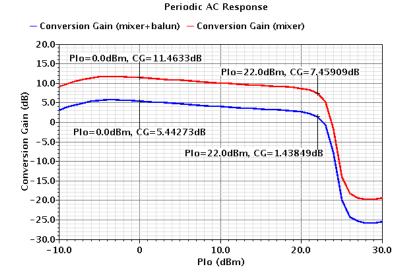


Fig. 6. Conversion gain (in dB) vs. PLO (with ideal L)

- Conversion Gain (mixer+balun) — Conversion Gain (mixer) 5.0 Plo=0.0dBm, CG=-4.94556dB Plo=22.0dBm, CG=-2.56747dB Plo=22.0dBm, CG=-8.58807dB Plo=0.0dBm, CG=-10.9662dB

Periodic AC Response

Fig. 7. Conversion gain (in dB) vs. P_{LO} (using ASITIC L)

10.0

Plo (dBm)

Based on the conversion gain simulation plots, input and output impedance matching contribute to better performance. Furthermore, using ideal inductors for impedance matching produced better performance as compared to using non-ideal ASITIC inductors through the n2port. It can be observed from the simulation plots that the conversion gain of the mixer only is higher than the conversion gain of the whole circuit consisting of the mixer and the balun. This is because the balun in the circuit, which is a passive balun, has insertion loss and thus

-10.0

incapable of producing gain. When a passive balun is cascaded with another block, for this case the mixer, the overall gain is degraded.

20.0

For the noise figure, Periodic Noise (Pnoise) analysis with PSS analysis is used. Alternatively, Periodic S-Parameters (PSP) analysis with PSS analysis can also be used to determine the noise figure of the circuit. Noise figure from a sweep range of -10dBm to 30dBm can now be determined and plotted using these analyses. The resulting plots are shown in Figs. 8-9.

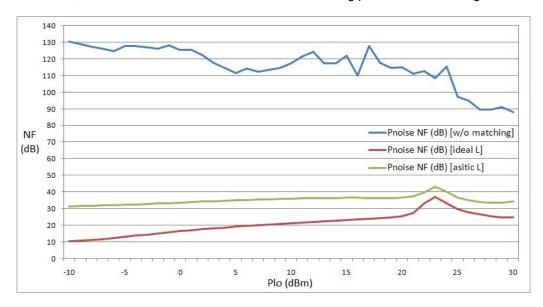


Fig. 8. Noise figure (in dB) vs. PLO of (Pnoise analysis)

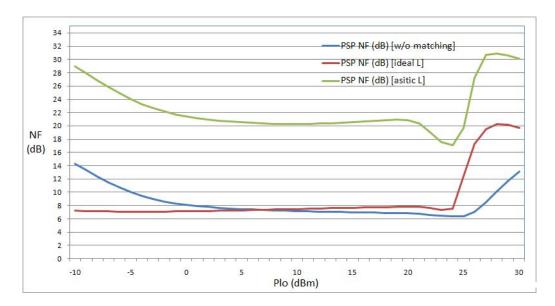


Fig. 9. Noise figure (in dB) vs. PLO of (PSP analysis)

Input and output impedance matching also contribute to better noise performance of the circuit, as indicated in Figs. 8-9. It can be observed that using ideal inductors for impedance matching produced lower noise figure as compared to using non-ideal ASITIC inductors through the n2port model. The model block n2port introduces noise to the system, hence, adding to the total noise figure of the circuit.

Table 5 summarizes the simulation results for conversion gain and noise figure at P_{LO} = 0dBm.

Table 5. Simulation results, at $P_{LO} = 0$ dBm

Figures of merit	Value
CG (mixer+balun) [w/o	-17.431dB
matching]	
CG (mixer) [w/o matching]	-11.410dB
CG (mixer+balun) [ideal L]	5.443dB
CG (mixer) [ideal L]	11.463dB
CG (mixer+balun) [ASITIC L]	-10.966dB
CG (mixer) [ASITIC L]	-4.946dB
Pnoise NF [w/o matching]	125.355dB
Pnoise NF [ideal L]	16.529dB
Pnoise NF [ASITIC L]	33.713dB
PSP NF [w/o matching]	8.127dB
PSP NF [ideal L]	7.136dB
PSP NF [ASITIC L]	21.437dB

It is evident that input and output impedance matching contribute to better performance based on the figures of merit presented for the Gilbertcell mixer design. It is observed that the conversion gain of the mixer is higher than the conversion gain of the circuit consisting of the mixer and the balun. The reason is that the conversion gain performance at the system-level perspective is greatly influenced by the performance of the initial or preceding blocks, for this case the passive balun. Hence, it is of high importance to consider the contribution of the input or previous circuit (and as well as the output or succeeding circuit) in fully designing and optimizing the mixer.

5. CONCLUSIONS AND RECOMMENDA-TIONS

A design of Gilbert-cell mixer with direct-conversion architecture was implemented and optimized on this paper. Conversion gain and noise figure were determined to gauge the performance of the mixer design. These performance parameters can still be enhanced or optimised by applying impedance matching in the circuit. The effect of the passive balun in the mixer design was also observed, resulting to the decrease in the conversion gain of the mixer. Nevertheless, the direct-conversion Gilbert-cell mixer design achieved conversion gain of 11.463dB and noise figure of 16.529dB using Pnoise analysis at 5GHz, comparable to mixer designs from past studies and research.

For future studies, active baluns could be used in place of passive baluns for monolithic implementation. Active baluns are capable of producing gain and if cascaded in a double-balanced mixer to supply the differential RF and

LO inputs, the overall performance of the mixer can be improved [6]. Although active baluns are unidirectional converters, they can be used for their large bandwidth, which is beyond from what non-ideal passive baluns can offer.

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COMPETING INTERESTS

Author has declared that no competing interests exist.

REFERENCES

- Razavi B. RF microelectronics. 2nd Ed. Upper Saddle River, New Jersey, USA: Prentice Hall Press; 2011.
- Zhou Y, Yoong CP, Weng LS, Khoi YJ, Wah MCY, Moy KAC, Fatt DWT. A 5 GHz dual-mode WiMAX/WLAN directconversion receiver. IEEE International Symposium on Circuits and Systems; 2006.
- Atallah JG, Rodriguez S, Zeng LR, Ismail M. A direct conversion WiMAX RF receiver front-end in CMOS technology. International Symposium on Signals, Circuits and Systems. 2007;1.
- Lee T. The design of CMOS radiofrequency integrated circuits. 2nd Ed. Cambridge: Cambridge University Press; 2003.
- Voltti M, Koivisto T, Tiiliharju E. Comparison of active and passive mixers.

- 18th European Conference on Circuit Theory and Design. 2007;890-893.
- Gomez FR, De Leon MT, Roque CR. Active balun circuits for WiMAX receiver front-end. TENCON 2010 – IEEE Region 10 Conference. 2010;1156-1161.
- 7. Tikka T, Ryynanen J, Hotti M, Halonen K. Design of a high linearity mixer for direct-conversion base-station receiver. IEEE International Symposium on Circuits and Systems; 2006.
- 8. Hamed KW, Freundorfer AP, Antar YMM. A monolithic double-balanced direct conversion mixer with an integrated wideband passive balun. IEEE Journal of Solid-State Circuits. 2005;40(3):622-629.
- 9. Park J, Lee CH, Kim BS, Laskar J. Design and analysis of low flicker-noise CMOS mixers for direct-conversion receivers. IEEE Transactions on Microwave Theory and Techniques. 2006;54(12).
- Gomez FR. Design of impedance matching networks for RF applications. Asian Journal of Engineering and Technology. 2018;6(4).
- Meyer RG, Niknejad AM. ASITIC for Windows NT/2000. Research in RFIC Design.
 - Available: http://rfic.eecs.berkeley.edu/~nik nejad/Asitic/grackle/cygwin_info.html
- Niknejad AM, Meyer RG. Analysis and optimization of monolithic inductors and transformers for RF ICs. IEEE Custom Integrated Circuits Conference, Santa Clara, CA. 1997;375-378.
- Stanford Microwave Integrated Circuits Laboratory. Integrated Spiral Inductor Calculator.
 - Available: http://www-smirc.stanford.edu/spiralCalc.html
- Mohan SS, del Mar Hershenson M, Boyd SP, Lee TH. Simple accurate expressions for planar spiral inductances. IEEE Journal of Solid-State Circuits. 1999;34(10):1419-1424.

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